**LEARN VERILOG/SYSTEM VERILOG**

Contents

[1. Data Types: 2](#_Toc55163274)

[2. Simulation Modeling: 2](#_Toc55163275)

[3. Building Blocks: 2](#_Toc55163276)

[a. Module: 2](#_Toc55163277)

[b. Ports: 2](#_Toc55163278)

[c. Initial block: 3](#_Toc55163279)

[d. Always block: 3](#_Toc55163280)

[Pitfalls: 3](#_Toc55163281)

[e. Always\_ff, always\_latch, always\_comb: 4](#_Toc55163282)

[f. Combinational/Sequential Circuits: 4](#_Toc55163283)

[g. Operators: 4](#_Toc55163284)

[h. Parameters: 4](#_Toc55163285)

[i. Generate: 5](#_Toc55163286)

[4. Control Flow: 5](#_Toc55163287)

[a. Blocking /Non-Blocking statements: 5](#_Toc55163288)

[b. Assign statement: 6](#_Toc55163289)

[c. If, For, while, do while statements: 6](#_Toc55163290)

[d. Case statements – case, casex, casez: 6](#_Toc55163291)

[e. Forever loop: 7](#_Toc55163292)

[f. Function, Task: 7](#_Toc55163293)

[5. System tasks/functions: 8](#_Toc55163294)

[a. Display tasks: 8](#_Toc55163295)

[b. Math functions: 8](#_Toc55163296)

[c. Timescale: 9](#_Toc55163297)

[6. Verilog scheduling region: 10](#_Toc55163298)

[7. Processes: 11](#_Toc55163299)

[8. Interface: 11](#_Toc55163300)

[9. Class: 11](#_Toc55163301)

[10. Constraints: 11](#_Toc55163302)

[11. Misc. constructs: 11](#_Toc55163303)

[12. Functional coverage: 11](#_Toc55163304)

[13. Assertions: 11](#_Toc55163305)

# Data Types:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Type** | **Size** | **2-state/4-state** | **Signed/Unsigned** | **C-Type** | **SV/Verilog** |
| wire | >=1 | 4 | Unsigned |  | Verilog/SV |
| Reg | >=1 | 4 | Unsigned |  | Verilog/SV |
| Integer | 32-bit | 4 | Signed |  | Verilog/SV |
| Real | 64 |  |  | Double | Verilog/SV |
| Time | 64 | 4 | Unsigned | Long int | Verilog/SV |
| Real Time | 64 |  |  | Double | Verilog/SV |
| Logic | >=1 | 4 | Unsigned |  | SV |
| Bit | >=1 | 2 | Unsigned |  | SV |
| Byte | 8 | 2 | Signed | Char | SV |
| Shortint | 16 | 2 | Signed | Short int | SV |
| Int | 32 | 2 | Signed | Int | SV |
| Longint | 64 | 2 | Signed | Long int | SV |
| Shortreal | 32 |  |  | Float | SV |

# Simulation Modeling:

* Gate Level AND(out,a,b);
* Behavior level out = a & b;
* Switch level nmos(out,d,cntrl);

# Building Blocks:

## Module:

module Adder();

…………………..

endmodule

Adder A0();

Adder A1();

## Ports:

Input, output, inout

Module Adder(

input a,

input b,

output out

);

Wire a0, b0;

Reg out0;

Adder A0(.a(a0), .b(b0), .out(out0));

## Initial block:

This is used to set initial values for simulation in test bench. Executes sequentially and non-synthesizable. You can have multiple initial blocks and all of them will be executed in parallel.

Initial being

a = ‘hACED;

#10;

$finish;

end

## Always block:

Always @ (event) being

…………………..

end

event: posedge; negedge; input or output

Will trigger when there is change in event. Can have multiple always blocks. If events are same in multiple blocks, all of them will trigger at same time and order cannot be guaranteed.

* Always make sure sensitive list is complete with statements being assigned in block.
* Always make sure all assignments happen irrespective of path in the block. Else latch will be implemented instead of flip flop.

### Pitfalls:

Always @(A) begin (In-correct)

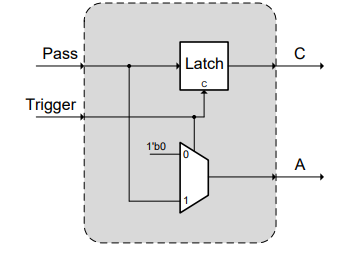
Out = A & B;

End

Always @(A, B) begin (Correct)

Out = A & B;

End

Always @ (\*) begin (In-correct)

A = 1’b0;

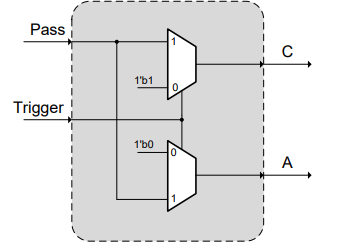
If (trigger) begin

A = pass;

C = pass;

end

end



Always @ (\*) begin (correct)

A = 1’b0;

C = 1’b0;

If (trigger) begin

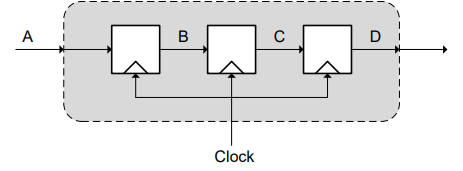
A = pass;

C = pass;

end

end

**Shift register:**

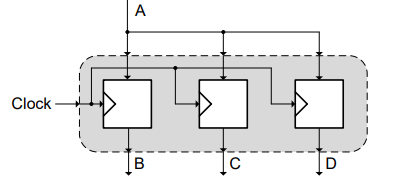
Always @ (\*) begin (correct)

B <= A;

C <= B;

D <= C;

End



Always @ (\*) begin (In-correct)

B = A;

C = B;

D = C;

end

## Always\_ff, always\_latch, always\_comb:

Always\_ff – uses only non-blocking statements and implements flip-flop.

Replaces always @(posedge).

Always\_latch – used to implement latch. Replaces always @ (\*)

Always\_comb - used to implement combinational circuits.

## Combinational/Sequential Circuits:

Combinational:

* Use Assign statements for combinational circuit. Cannot contain any storage elements like reg, clk etc.
* Always block can also be used for combinational.

Sequential:

* Should contain always blocks with clk as event.
* Storage elements must be present as reg/logic etc.

## Operators:

Most of the operators are same as C-style.

A === B; A should be equal to B including X, Z states

A!==B; A should not be equal to B including X, Z states

A == B; A should be equal to B, excluding X, Z states

## Parameters:

Global: parameter MSB = 7;

Module:

Module sum (a, b, out);

Parameter BUS\_WIDTH = 32, DATA\_WIDTH = 64;

Endmodule

(or)

Module sum #(parameter BUS\_WIDTH =32, parameter DATA\_WIDTH = 64) (a, b, out);

Endmodule

Module tb;

Sum s0 #(BUS\_WIDTH = 64, DATA\_WIDTH = 128) ([port\_list]);

Endmodule

## Generate:

Used to instantiate a module multiple times.

// Design for a half-adder

module ha ( input a, b,

output sum, cout);

assign sum = a ^ b;

assign cout = a & b;

endmodule

// A top level design that contains N instances of half adder

module my\_design

#(parameter N=4)

( input [N-1:0] a, b,

output [N-1:0] sum, cout);

// Declare a temporary loop variable to be used during

// generation and won't be available during simulation

genvar i;

// Generate for loop to instantiate N times

generate

for (i = 0; i < N; i = i + 1) begin

ha u0 (a[i], b[i], sum[i], cout[i]);

end

endgenerate

endmodule

module tb;

parameter N = 2;

// Instantiate top level design with N=2 so that it will have 2

// separate instances of half adders and both are given two separate inputs

my\_design #(.N(N)) md( .a(a), .b(b), .sum(sum), .cout(cout));

endmodule

# Control Flow:

## Blocking /Non-Blocking statements:

“=” Blocking statement and execute in sequence;

“<=” Non-blocking statement and execute in parallel.

a = #10 1’b1; a = 1 @ time 10

b = #20 1’b0; b = 0 @ time 30

c <= #10 ‘hACED; c = ACED @ time 10

d <= #5 ‘hDEAD; d = DEAD @ time 5

## Assign statement:

This can be used only for non-storage elements as wire, logic etc.

## If, For, while, do while statements:

Same as c-style.

## Case statements – case, casex, casez:

? – wildcard or don’t care

casex: X, Z are don’t cares

casez: Z is don’t care.

**Example:**

initial begin

#1 $display ("\n Driving 0");

sel = 0;

#1 $display ("\n Driving 1");

sel = 1;

#1 $display ("\n Driving x");

sel = 1'bx;

#1 $display ("\n Driving z");

sel = 1'bz;

#1 $finish;

end

always @ (sel)

case (sel)

1'b0 : $display("Normal : Logic 0 on sel");

1'b1 : $display("Normal : Logic 1 on sel");

1'bx : $display("Normal : Logic x on sel");

1'bz : $display("Normal : Logic z on sel");

endcase

always @ (sel)

casex (sel)

1'b0 : $display("CASEX : Logic 0 on sel");

1'b1 : $display("CASEX : Logic 1 on sel");

1'bx : $display("CASEX : Logic x on sel");

1'bz : $display("CASEX : Logic z on sel");

endcase

always @ (sel)

casez (sel)

1'b0 : $display("CASEZ : Logic 0 on sel");

1'b1 : $display("CASEZ : Logic 1 on sel");

1'bx : $display("CASEZ : Logic x on sel");

1'bz : $display("CASEZ : Logic z on sel");

endcase

**Result:**

Driving 0

Normal: Logic 0 on sel

CASEX: Logic 0 on sel

CASEZ: Logic 0 on sel

Driving 1

Normal: Logic 1 on sel

CASEX: Logic 1 on sel

CASEZ: Logic 1 on sel

Driving x

Normal : Logic x on sel

CASEX : Logic 0 on sel

CASEZ: Logic x on sel

Driving z

Normal: Logic z on sel

CASEX: Logic 0 on sel

CASEZ: Logic 0 on sel

## Forever loop:

Forever begin

@ (posedge clk) begin

………………

end

end

## Function, Task:

**Function [automatic] [return\_type] name ([port\_list]);**

**Endfunction**

Function [7:0] sum;

Input [7:0] a, b;

Begin

Sum = a +b;

end

endfunction

(or)

Function [7:0] sum (input [7:0] a, b);

Begin

Sum = a +b;

End

Endfunction

* Automatic is used for dynamically allocate rather than share between invocations.
* Functions cannot have time-controlled statements as #, @, wait, posedge, negedge
* Should have at least one input
* Cannot have non-blocking assignments, force-release, assign-deassign
* Cannot have output, inout, triggers
* Can call other functions but not task
* Can return a single value

Task [name];

Input [port\_list];

Output [port\_list];

Inout [port\_list];

Begin

…………

End

Endtask

Task [name] (input [port\_list], inout [port\_list], output [port\_list]]);

Begin

……….

End

Endtask

Task [name] ();

Begin

………..

End

Endtask

* Automatic is used for dynamically allocate rather than share between invocations.
* Can have time-controlled statements
* Can have/not have input, inout, output
* Cannot return a value, but can achieve using output
* Can call tasks or functions

Global tasks:

Task display ();

…………

Endtask

* Global task can be outside of module
* Disable can be used using “disable” keyword

# System tasks/functions:

## Display tasks:

* $display: Appends new line
* $strobe: Final value of variable at end of current delta time-step
* $write: Doesn’t append new line
* $monitor: Prints whenever variable changes

|  |  |
| --- | --- |
| %h, %H | Display in hexadecimal format |
| %d, %D | Display in decimal format |
| %b, %B | Display in binary format |
| %m, %M | Display hierarchical name |
| %s, %S | Display as a string |
| %t, %T | Display in time format |
| %f, %F | Display 'real' in a decimal format |
| %e, %E | Display 'real' in an exponential format |

## Math functions:

|  |  |
| --- | --- |
| $ln(x) | Natural logarithm log(x) |
| $log10(x) | Decimal Logarithm log10(x) |
| exp(x) | Exponential of x (ex) where e=2.718281828... |
| sqrt(x) | Square root of x |
| $pow(x, y) | xy |
| $floor(x) | Floor x |
| $ceil(x) | Ceiling x |
| $sin(x) | Sine of x where x is in radians |
| $cos(x) | Cosine of x where x is in radians |
| $tan(x) | Tangent of x where x is in radians |
| $asin(x) | Arc-Sine of x |
| $acos(x) | Arc-Cosine of x |
| $atan(x) | Arc-tangent of x |
| $atan2(x, y) | Arc-tangent of x/y |
| $hypot(x, y) | Hypotenuse of x and y : sqrt(xx + yy) |
| $sinh(x) | Hyperbolic Sine of x |
| $cosh(x) | Hyperbolic-Cosine of x |
| $tanh(x) | Hyperbolic-Tangent of x |
| $asinh(x) | Arc-hyperbolic Sine of x |
| $acosh(x) | Arc-hyperbolic Cosine of x |
| $atanh(x) | Arc-hyperbolic tangent of x |

## Timescale:

**`timescale <time\_unit/time\_precision>**

initial begin

val <= 0; // Initialize the signal to 0 at time 0 units

#1 $display ("T=%0t at time #1", $realtime); // Advance by 1-time unit, disp msg and toggle val

val <= 1;

#0.49 $display ("T=%0t at time #0.49", $realtime); // Advance by 0.49-time unit and toggle val

val <= 0;

#0.50 $display ("T=%0t at time #0.50", $realtime); // Advance by 0.50-time unit and toggle val

val <= 1;

#0.51 $display ("T=%0t at time #0.51", $realtime); // Advance by 0.51-time unit and toggle val

val <= 0;

#5 $display ("T=%0t End of sim", $realtime); // Let sim run for another 5 time units and exit

End

**`timescale 1ns/1ns**

T=1 At time #1

T=1 At time #0.49

T=2 At time #0.50

T=3 At time #0.51

T=8 End of simulation

**`timescale 1ns/1ps**

T=1000 At time #1

T=1490 At time #0.49

T=1990 At time #0.50

T=2500 At time #0.51

T=7500 End of simulation

**`timescale 10ns/1ns**

T=10 At time #1

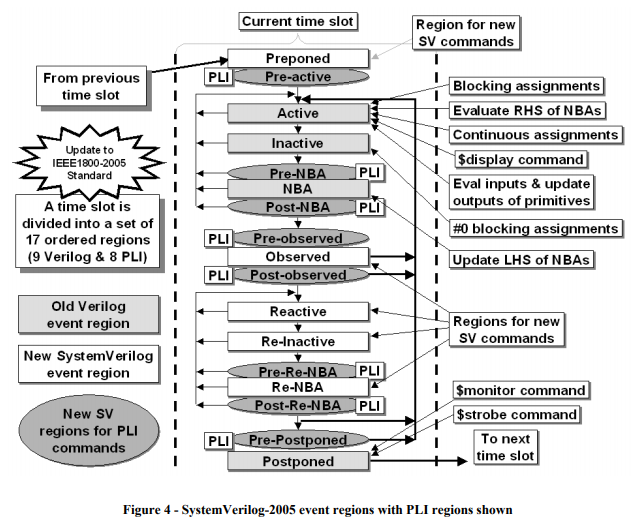
T=15 At time #0.49

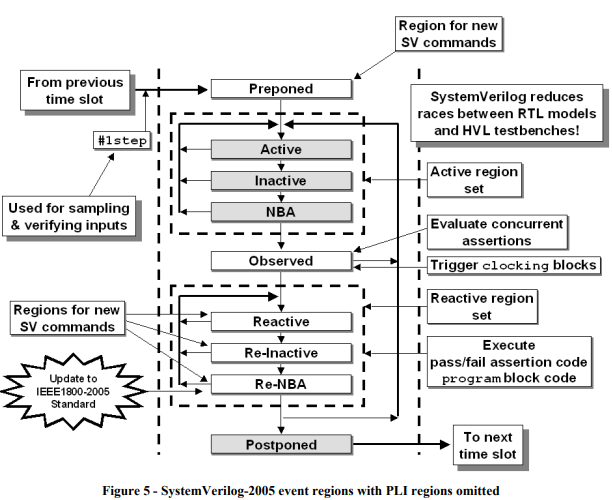
T=20 At time #0.50

T=25 At time #0.51

T=75 End of simulation

# Verilog scheduling region:





# Processes:

# Interface:

# Class:

# Constraints:

# Misc. constructs:

# Functional coverage:

# Assertions: